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Date 8/28/03 Serial # 10/022,297 Priority Application Date 12/14/00

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1, 4-16, 18-26 (Independent 1, 4, 8-12)

Problem: See Page 2 Paragraph 2

" " 3 " P-10

Solution: " " " " 11-13

Please look for the specific materials utilized (For ex: See Paragraphs 37-57, for the substrate, ink and resin)

Staff Use Only	Type of Search	Vendors
Searcher: Bode ?	Structure (#)_____	STN_____
Searcher Phone: 605-1426	Bibliographic ✓	Dialog ✓
Searcher Location: STIC-EIC2800, CP4-9C18	Litigation_____	Questel/Orbit_____
Date Searcher Picked Up: 09-02-03	Fulltext_____	Lexis-Nexis_____
Date Completed: 09-02-03	Patent Family_____	WWW/Internet_____
Searcher Prep/Rev Time: 40	Other_____	Other_____
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AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions of the claims and any prior listing of the claims in the present application. In the following listing, Claim 17 is canceled herein without prejudice, and Claims 2 and 3 were previously canceled. Claims 5, 8, 13, 16, 18-20 and 22 are amended herein. Claims 1, 4, 6, 7, 9-12, 14, 15, 21 and 23-26 remain as originally filed or as previously amended.

Claim 1 (Previously Amended): A semiconductor device comprising a substrate, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer only through which the semiconductor chip is joined with the land, and a synthetic resin covering the land, the solder layer and the semiconductor chip on the substrate, a coefficient of expansion of the synthetic resin being generally less than a coefficient of expansion of the substrate or a coefficient of expansion of the land.

Claim 2 (Previously Canceled)

Claim 3 (Previously Canceled)

Claim 4 (Previously Amended): A semiconductor device comprising a substrate, the substrate comprising aluminum, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer only through which the semiconductor chip is joined with the land, and a synthetic resin covering the land, the solder layer and the semiconductor chip on the substrate, a coefficient of expansion of the synthetic resin being generally less than a coefficient of expansion of aluminum.

Claim 5 (Currently Amended): The semiconductor device as set forth in Claim 4, wherein the coefficient of the ~~linear~~ expansion of the synthetic resin is generally less than approximately 23 ppm/°K.

Claim 6 (Previously Amended): The semiconductor device as set forth in Claim 4, wherein the land comprises copper.

Claim 7 (Previously Amended): The semiconductor device as set forth in Claim 4, wherein the synthetic resin includes epoxide.

Claim 8 (Currently Amended): A semiconductor device comprising a substrate, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer only through which the semiconductor chip is joined with the land, and a synthetic resin ~~covering~~ that covers the land, the solder layer and the semiconductor chip on the substrate, ~~a coefficient of expansion of~~ the synthetic resin having a coefficient of expansion, the coefficient of expansion of the synthetic resin being generally less than a larger one of a coefficient of expansion of the substrate and a coefficient of expansion of the land, and the coefficient of expansion of the resin being generally greater than ~~the other~~ a smaller one of the coefficient of expansion of the substrate and the coefficient of expansion of the land.

Claim 9 (As Originally Filed): The semiconductor as set forth in Claim 8, wherein the coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the substrate and is greater than the coefficient of expansion of the land.

Claim 10 (As Originally Filed): The semiconductor as set forth in Claim 8, wherein the coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the land and is greater than the coefficient of expansion of the substrate.

Claim 11 (As Originally Filed): The semiconductor as set forth in Claim 8, wherein the substrate comprises aluminum.

Claim 12 (As Originally Filed): The semiconductor device as set forth in Claim 11, wherein the coefficient of the expansion of the synthetic resin is generally less than a coefficient of expansion of aluminum.

Claim 13 (Currently Amended): The semiconductor device as set forth in Claim 1, wherein the semiconductor chip defines at least two corners positioned generally opposite to each other, the land has an outer boundary that defines at least two ~~corners~~ corner portions in proximity to the

corners of the semiconductor chip, the outer boundary further defines contiguous portions extending next to the corner portions and spaced apart from the semiconductor chip more than the corner portions, and the ~~corners~~ corner portions of the land generally confine the corners of the semiconductor chip therein.

Claim 14 (As Originally Filed): The semiconductor device as set forth in Claim 1, wherein the semiconductor chip controls electric power.

Claim 15 (As Originally Filed): The semiconductor device as set forth in Claim 14, wherein the semiconductor chip controls power of an electric motor arranged to drive an electric vehicle.

Claim 16 (Currently Amended): A semiconductor device comprising a substrate, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer joining the semiconductor chip with the land, the semiconductor chip defining at least two corners positioned generally opposite to each other, the land having an outer boundary defining at least two ~~corners~~ corner portions disposed in proximity to the corners of the semiconductor chip, the outer boundary further defining contiguous portions extending next to the corner portions and spaced apart from the semiconductor chip more than the corner portions, the ~~corners~~ corner portions of the land generally confining the corners of the semiconductor chip therein.

Claim 17 (Currently Canceled)

Claim 18 (Currently Amended): The semiconductor device as set forth in Claim 16, wherein the semiconductor chip is generally configured as a ~~rectangular~~ shape having at least one diagonal line, and the corners of the semiconductor chip are positioned on ~~a~~ the diagonal line of the ~~rectangular~~ shape.

Claim 19 (Currently Amended): The semiconductor device as set forth in Claim 18, wherein the semiconductor chip defines four corners, and the land defines four ~~corners~~ corner portions corresponding to the corners of the semiconductor chip.

Claim 20 (Currently Amended): The semiconductor device as set forth in Claim 18, wherein the semiconductor chip is generally configured as a rectangular shape, and wherein at least a length of a shorter side of the rectangular shape is longer than approximately 2.5 millimeters.

Claim 21 (Currently Amended): The semiconductor device as set forth in Claim 16, wherein the land is generally configured as a rectangular shape except for the ~~corners~~ corner portions.

Claim 22 (Currently Amended): The semiconductor device as set forth in Claim 16, wherein the land is generally configured as a round shape except for the ~~corners~~ corner portions.

Claim 23 (As Originally Filed): The semiconductor as set forth in Claim 16, wherein an area of the land is larger than an area of the semiconductor chip, and the area of the land generally shrinks toward the corners of the semiconductor chip.

Claim 24 (As Originally Filed): The semiconductor as set forth in Claim 16, wherein an area of the land is larger than an area of the semiconductor chip, and the area of the land generally expands from the corners of the semiconductor chip.

Claim 25 (As Originally Filed): The semiconductor device as set forth in Claim 16, wherein the semiconductor chip controls electric power.

Claim 26 (As Originally Filed): The semiconductor device as set forth in Claim 16, wherein the semiconductor chip is joined with the land in a reflow soldering method.

Claims 27-32 (Previously Canceled)

SEMICONDUCTOR DEVICE FOR POWER CONTROL

Priority Information

[0001] This application is based on and claims priority to Japanese Patent Application No. 2000-379567, filed December 14, 2000, Japanese Patent Application No. 2000-379569, filed December 14, 2000, and Japanese Patent Application No. 2001-052498, filed February 27, 2001, the entire contents of which are hereby expressly incorporated herein by reference.

Background of the Invention

Field of the Invention

[0002] The present invention relates to a semiconductor device and, more particularly, relates to an improved semiconductor device for power control in which a semiconductor chip is mounted on a substrate.

Description of Related Art

[0003] Semiconductor devices are utilized in wide variety of technical areas. For instance, a motor controller for an electrically operated vehicle such as, for example, an electric golf cart, includes a semiconductor device for power control of a motor that drives the golf cart. Typically, the semiconductor device that controls electric power is provided with one or more semiconductor chips that allow a relatively large current to flow therethrough. Because of the nature of power controlling semiconductor chips, the device can build much heat therein and needs a heat radiation structure. Thus, the semiconductor chips normally are placed on metallic heat spreaders that are mounted on metallic lands, which are formed on a metallic substrate, to expedite radiation of the heat. The heat spreaders are soldered onto the lands. The semiconductor chips are soldered onto the heat spreaders. Meanwhile, since a vehicle (for example, a golf cart) typically is used outdoors, the semiconductor device is exposed to a wet or dusty environment that can cause malfunctions of the device. In order to prevent the malfunctions from occurring, synthetic resin can be employed to entirely cover the semiconductor chips together with the lands.

[0004] FIGURES 1 and 2 schematically illustrate typical structures of a semiconductor device 10. A base metal 20 is coated with dielectric or insulating 22 to form a metallic substrate 24. Patterns of metallic lands 26 are formed on an upper surface of the substrate 24. Semiconductor chips 28 are joined to the metallic lands 26 via heat spreaders 30. More specifically, the semiconductor chips 28 are soldered onto the heat spreaders 30 with a solder layer 32 that has a relatively high melting point, and the heat spreaders 30 are then soldered onto the lands 26 with another solder layer 34 that has a relatively low melting point. Bonding wire pads 36 also are formed on the substrate 24 and are connected with the respective semiconductor chips 28 through bonding wires 38. After completion of the soldering and bonding processes, a synthetic resin 40 covers all the elements on the substrate 24.

[0005] FIGURE 1 shows an example of the semiconductor device 10 that uses silicone gel for the synthetic resin 40. Because the viscosity of the silicone gel is relatively small, side walls 42 are applied to prevent the silicone gel from spilling before hardening. FIGURE 2 shows another example of the semiconductor device 10 that uses epoxide. No side walls are necessary in this example because the epoxide has sufficient viscosity to stay on the substrate 24.

[0006] The heat spreaders 30 not only expedite radiation of the heat accumulating in the semiconductor chips 28 but also relieve the heat stress caused by disparity between the respective coefficients of the semiconductor chips 28 and the substrate 24. That is, the heat spreaders 30 cause the difference between the thermal expansion (or contraction) magnitude of the semiconductor chips 28 and the substrate 24 to be small. Accordingly, cracks of the solder layers 32, 34 or the semiconductor chips 28 and peeling of the semiconductor chips 28 from the solder layers 32, 34 are effectively prevented.

[0007] The usage of the heat spreaders 30, however, increases the number of parts, makes the semiconductor devices complicated and bulky, and increases the number of manufacturing processes. In addition, because the heat spreaders 30 are larger than the semiconductor chips 28, the lands 26 are inevitably large and require relatively wide spaces for them. Thus, the packaging density of the semiconductor chips 28 on the substrate 24 is diminished. A large casing that occupies a large area and has a large capacity may be necessary to accommodate the semiconductor chip 28.

[0008] A need therefore exists for an improved semiconductor device that has sufficient packaging density to make the device compact enough.

[0009] As thus far described, the soldering process is necessary for fixing the semiconductor chips onto the substrate. Several tools can be applied to hold the semiconductor chips in accurate positions, or each semiconductor chip can be soldered one by one for the same purpose. Both methods, however, need a number of steps and increase production cost accordingly.

[0010] Another need thus exists for an improved semiconductor device that can hold high accuracy of positioning of semiconductor chips without requiring expensive production cost.

Summary of the Invention

[0011] In accordance with one aspect of the present invention, a semiconductor device comprises a substrate. A land is formed on the substrate. A semiconductor chip is mounted on the land. A solder layer is provided only through which the semiconductor chip is joined with the land. A synthetic resin covers the land, the solder layer and the semiconductor chip on the substrate.

[0012] In accordance with another aspect of the present invention, a semiconductor device comprises a substrate. A land is formed on the substrate. A semiconductor chip is mounted on the land. A solder layer joins the semiconductor chip with the land. The semiconductor chip defines at least two corners positioned generally opposite to each other. The land defines at least two corners disposed in proximity to the corners of the semiconductor chip. The corners of the land generally confine the corners of the semiconductor chip therein.

[0013] In accordance with a further aspect of the present invention, a method for joining a semiconductor chip to a substrate comprises forming a land on the substrate, soldering the semiconductor chip directly to the land, and covering the land and the semiconductor chip with a synthetic resin.

Brief Description of the Drawings

[0014] These and other features, aspects and advantages of the present invention will now be described with reference to the drawings of preferred embodiments which are intended to illustrate and not to limit the invention. The drawings comprise 26 figures.

[0015] As noted above, FIGURES 1 and 2 illustrate schematic views of conventional semiconductor devices. The figures are provided in order to assist in understanding the conventional arrangements and for comparison with the aspects, features and advantages associated with the present invention.

[0016] FIGURE 3 is a circuit diagram of a motor controller for an electric golf cart that includes a semiconductor device configured in accordance with a preferred embodiment of the present invention.

[0017] FIGURE 4 is a plan view of the semiconductor device.

[0018] FIGURE 5 is a front elevational view of the semiconductor device.

[0019] FIGURE 6 is a top plan view of the motor controller without a casing.

[0020] FIGURE 7 is a front elevational view of the motor controller without a casing.

[0021] FIGURE 8 is a side view of the motor controller without a casing viewed from a location on the right hand side.

[0022] FIGURE 9 is a plan view of a terminal bar for the motor controller.

[0023] FIGURE 10 is a front elevational view of the terminal bar.

[0024] FIGURE 11 is a plan view of the motor controller with a casing.

[0025] FIGURE 12 is a front elevational view of the motor controller with the casing.

[0026] FIGURE 13 is side view of the motor controller with the casing viewed from a location on the right hand side.

[0027] FIGURE 14 is a schematic front view of the semiconductor device that corresponds to the semiconductor device of FIGURE 5.

[0028] FIGURE 15 is a schematic, partial top plan view of the semiconductor device that has a land pattern configured in accordance with a preferred arrangement of the present invention.

[0029] FIGURE 16 is a schematic, partial top plan view of the semiconductor device that has a modified land pattern.

[0030] FIGURE 17 is a schematic, partial top plan view of the semiconductor device that has a further modified land pattern.

[0031] FIGURE 18 is a schematic, partial top plan view of the semiconductor device that has a still further modified land pattern.

[0032] FIGURE 19 is a schematic, partial side view of the semiconductor device viewed from the line 19-19 of FIGURE 15.

[0033] FIGURE 20 is a flow chart showing production processes of the semiconductor device illustrated in FIGURES 15-19.

[0034] FIGURE 21 is a flow chart illustrating other production processes of the semiconductor device.

[0035] FIGURE 22 is a flow chart illustrating further production processes of the semiconductor device.

[0036] FIGURE 23 is a schematic top plan view of the semiconductor device with a mounting tool used for practicing the production processes shown in FIGURE 22.

[0037] FIGURE 24 is a schematic front elevational view of the semiconductor device of FIGURE 23 with the tool.

[0038] FIGURE 25 is an enlarged sectional view of the semiconductor device of FIGURE 23 with the tool.

[0039] FIGURE 26 is a top plan view of the semiconductor device of FIGURE 23 without the tool.

Detailed Description of the Preferred Embodiments

[0040] An overall construction of a motor controller 50 for an electric is described below with reference to FIGURES 3-13. The motor controller 50 includes a semiconductor device 52 configured in accordance with certain features, aspects and advantages of the present invention. The electric vehicle can be, for example, an electric golf cart, and the motor controller 50 can be an apparatus for controlling electric power supplied to a DC motor 54 of the golf cart. The motor controller 50, however, merely exemplifies one of apparatuses that can employ the semiconductor device 52. The golf cart also is only an example. The semiconductor device can be applied to other apparatuses and machines including other electrically powered vehicles, and can be used for other purposes in addition to power control. The apparatuses, machines, vehicles and

purposes may be readily recognized along the spirit and scope of the invention, as defined by the appended claims.

[0041] With reference to FIGURE 3, the motor controller 50, which includes the semiconductor device 52, is connected with the DC motor 54, a battery 58 and a speed control circuit 60 to supply electric power to the motor 54 from the battery 58 under control of the speed control circuit 60. More specifically, the motor controller 50 is a chopper type, DC motor power control apparatus. The battery 58 is coupled with a pair of terminal bars 62A, 62B of the motor controller 50. A smoothing capacitor 64 is disposed between the terminal bars 62A, 62B and is electrically connected in parallel with the battery 58 to reduce voltage ripples.

[0042] The semiconductor device 52 preferably comprises three field effect transistors (FETs) 66 and three diodes 68. The drains D of the respective FETs 66 are connected with a first terminal of the motor 54 so that the FETs 66 are arranged in parallel to each other in the circuit. The cathodes K of the respective diodes 68 are connected to a second terminal of the motor 54. The anodes A of the diodes 68 are connected to the respective drains D of the FETs 66 and to the first terminal of the motor 54. Thus, the diodes 68 are arranged in parallel to each other.

[0043] An output terminal of the speed control circuit 60 is connected to respective gates of the FETs 66. The operator of the golf cart can change voltage levels of the speed control circuit 60 by operating a control mechanism such as, for example, an accelerator pedal. The speed control circuit 60 controls the rotational speed or torque of the motor 54.

[0044] The FETs 66 are selectively turned on by the voltage level from the speed control circuit 60. Duty ratios, (i.e., duty cycles) of the FETs 66 are altered to control current that flows through the motor 54. Meanwhile, when one or more FETs 66 are turned off, the current circulates through the associated diodes 68. By contiguous alteration of the duty ratios of the FETs 66 under control of the speed control circuit 60, the rotational speed of the motor 54 can be smoothly changed.

[0045] As shown in FIGURES 4 and 5, the illustrated semiconductor device 52 includes a printed wiring board 72. As used in the following description, the printed wiring board 72 may also be referred to as a metallic substrate or a substrate unless indicated otherwise or otherwise readily apparent from the context. The substrate 72

preferably is made of aluminum and has a rectangular shape. The FETs 66 and the diodes 68 are soldered onto the metallic substrate 72. Preferably, an insulating layer is formed on the substrate 72 by a surface treatment process prior to the soldering process. A circuit pattern is printed on the surface of the board 72. The FETs 66 and the diodes 68 are arranged in compliance with the pattern. A plurality of bonding wire pads 76 also are formed on the substrate 72. The FETs 66 and the diodes 68 are connected to the wire pads 76 by bonding wires 78. The FETs 66, the diodes 68, the wire pads 76 and the bonding wires 78 are covered with a synthetic resin 80 such as, for example, epoxide. Additionally, a plurality of pin connectors 82, which are connected with the respective FETs 66, extend upwardly from the printed wiring board or substrate 72. The printed wiring board 72 defines four openings 84 at four corners thereof.

[0046] As shown in FIGURES 6-8, a circuit board 88 is mounted on the printed wiring board 72. The circuit board 88 is approximately half the size of the printed wiring board 72. The circuit board 88 defines apertures 90 in which the pin connectors 82 are fitted. The pin connectors 82 and one or more spacers 92 support the circuit board 88 on the printed wiring board 72. The pin connectors 82 can be connected with the speed control circuit 60. The terminal bars 62A, 62B are affixed to the printed wiring board 72 by rivets 94 via insulators (not shown) and extend upwardly from the printed wiring board 72 next to the circuit board 88.

[0047] As shown in FIGURES 9 and 10, the terminal bar 62A, for example, preferably comprises copper plate and is shaped generally as an S-configuration. The terminal bar 62A comprises a bottom horizontal section 96A, a vertical section 98A and a top horizontal section 100A. The bottom section 96A preferably defines two apertures 102A. The printed wiring board 72 also defines two apertures 103A (FIGURE 5) corresponding to the apertures 102A of the bar 62A. The rivets 94 pass through the apertures to couple the bottom section 96A with the printed wiring board 72. The vertical section 98A defines an aperture 104A. The top section 100A defines an aperture 105A. The terminal bar 62B preferably comprises the same material, is shaped in substantially the same configuration, and has similar apertures. Since the terminal bar 62B is similar to the terminal bar 62A except for its size and except for the positions of the apertures, the same reference numerals are assigned to corresponding portions of the terminal bar 62B but with the letter B. Because the sizes of the respective terminal bars 62A, 62B and the

positions of the apertures 104A, 104B, 105A, 105B are shown in FIGURES 6-8, further descriptions about the sizes and the positions are not deemed necessary. Note that the bottom apertures (not shown) of the terminal bar 62B are positioned to match the apertures 103B in FIGURE 5.

[0048] The capacitor 64 has a pair of terminals 106 that are disposed on the same side and are formed with threaded holes. Two bolts 108 are fitted into the apertures 104A, 104B of the respective terminal bars 62A, 62B and are further fitted into the threaded holes of the terminals 106. Thus, the vertical sections 98A, 98B of the terminal bars 62A, 62B together support the capacitor 64. A pair of power cables can be connected with the respective apertures 105A, 105B to couple the terminal bars 62A, 62B with the battery 58.

[0049] Another terminal bar 62C, which is similar to the terminal bars 62A, 62B, is affixed to the printed wiring board 72 below the circuit board 88. Although the terminal bar 62C only has a nominal vertical section and no aperture is provided in the vertical section, the same reference numerals are assigned to the corresponding portions but with the letter C. Note that the bottom apertures (not shown) of the terminal bar 62C are positioned to match the aperture 103C in FIGURE 5. The terminal bar 62C is connected with the drains D of the FETs 66. A power cable can be connected with the aperture 105C to couple the terminal bar 62C with the motor 54.

[0050] Although not shown in FIGURES 6-8, the speed control circuit 60 (FIGURE 3) can be disposed on the circuit board 88. The speed control circuit 60 is connected to a potentiometer that is provided at the control mechanism through plurality of signal lines 112, which are tied together by a tubular member 114.

[0051] As shown in FIGURES 11-13, a protective casing 120 encloses the motor controller 50. The casing 120 preferably is made of aluminum and is configured generally as a rectangular parallelepiped tubular shape except for one top corner portion. Although any method can be used to produce the casing 120, either an extrusion molding process or a die-cast molding process is the most suitable method.

[0052] The entire body of the controller 50, except for the terminal bars 62A, 62B, 62C and the tubular member 114, is accommodated within the casing 120. A bottom portion 122 of the casing 120 has openings corresponding to the openings 84 of the printed wiring board 72. The printed wiring board 72 thus is affixed to the bottom

portion 122 by rivets through the openings. The bottom portion 122 has flanges 124 that extend along both lateral sides. The flanges 124 also define openings 126 through which bolts can pass to mount the casing onto an appropriate location of the golf cart. Top and lateral surfaces of the casing 120 form a plurality of grooves (or projections) 128 extending in parallel to each other and along the flanges 124. The grooves (or projections) 128 advantageously increase the surface area of the casing 120 to expedite radiation of heat from the casing 120. Within the casing 120, the space that is not occupied by the motor controller 50 is filled with synthetic resin. Although the synthetic resin 130 can be the same as the synthetic resin 80, a lower grade resin than the resin 80 (FIGURES 4 and 5) can be sufficient enough to fill the space.

[0053] As thus described, the FETs 66 and the diodes 68 are directly joined to the metallic substrate 72 that is fixed to the protective casing 120 without any specific heat radiator. Many parts, elements and members can be omitted, and the casing 120 can be extremely compact. Since the motor controller 50 is completely enclosed in the synthetic resin 130 and is firmly coupled with the casing 120 by the resin 130, condensation, dust and vibration cannot harm the motor controller 50.

[0054] As shown in FIGURE 14, the structure of the semiconductor device 52 will now be described in greater detail below.

[0055] The metallic substrate 72 preferably comprises a base metal 140 coated with a dielectric or insulating layer 142. Preferably the base metal 140 comprises aluminum, which has a coefficient of linear expansion of approximately 23 ppm/°K. Patterns of metallic lands 144 are printed on the insulating layer 142. The lands 144 preferably comprise copper, which has a coefficient of linear expansion of approximately 16-17 ppm/°K. As used in this description, the terms "aluminum," and "copper" include aluminum alloy and copper alloy, respectively. The semiconductor chips 66, which are FETs in the illustrated embodiment, are directly soldered onto the lands 144 by solder 146 without any intervening substances such as the conventional heat spreaders. Patterns of the wire bonding pads 76 also are printed on the insulating layer 142 and are connected to the respective semiconductor chips 66 through the bonding wires 78. After completion of the soldering and bonding processes, the synthetic resin 80 covers the lands 144, the semiconductor chips 66, the solder layer 146, the bonding pads 76 and the bonding wires

78. In other words, the synthetic resin 80 completely encloses all the elements on the substrate 72 therein.

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[0056] It has been found in experiments that cracks of the solder layer 146 or the FETs 66 (i.e., the semiconductor chips) and peeling of the FETs 66 from the solder layer 146 are effectively prevented without the conventional heat spreaders if the synthetic resin 80 at least meets the following condition. Preferably, the synthetic resin 80 is epoxide that has a coefficient of linear expansion generally less than 23 ppm/°K. The resin under this condition effectively relieves the thermal stress affected to the solder layer 146. Other synthetic resins may be used instead of the epoxide, but the resin should have a coefficient of linear expansion less than the coefficient of linear expansion of the lands 144 or the coefficient of linear expansion of the semiconductor chip (i.e., the FET 66) in order to produce the beneficial effect described above. In other words, the coefficient of linear expansion of the resin is generally less than one of the coefficient of linear expansion of the substrate 72 and the coefficient of linear expansion of the lands 144, and the coefficient of linear expansion of the resin is generally greater than the other one of the coefficient of linear expansion of the substrate 72 and the coefficient of linear expansion of the lands 144. Adjustment of the proportions of the components of the synthetic resin can produce the desired coefficient of linear expansion. No side walls are necessary if the epoxide is applied because the epoxide has sufficient viscosity. Materials other than aluminum or copper can be used for the substrate or the lands inasmuch as the foregoing condition is met.

[0057] Various methods such as, for example, a reflow soldering method or a die bonding method can be used to produce the semiconductor device 52. In the reflow soldering method, cream solder or half-solid solder is applied on all the lands 144 simultaneously. Then, the semiconductor chips 66 are placed on the respective lands 144 by, for example, a chip mounter. The substrate 72 with the semiconductor chips 66 placed on the lands 144 by the cream solder is put into a reflow furnace. The furnace generates a hot blast therein that reflows and then hardens the solder to firmly fix the semiconductor chips 66 onto the lands 144. The wire bonding pads 76 can be printed on the substrate 72 at the same time as the lands 144 are printed or later in another process. In either case, the wires 78 are bonded between the semiconductor chips 66 and the wire bonding pads 76 afterwards. Finally, the synthetic resin 80, which is the epoxide that has

the selected coefficient of linear expansion, is injected by a resin dispenser onto the substrate 72 on which the semiconductor chips 66 are joined. In the die bonding method, the semiconductor chips 66 are placed and soldered onto the lands 144 one by one. A wire bonding process follows each placing and soldering process and thus is done also one by one. Other processes are substantially the same as the processes in the reflow soldering method.

[0058] As thus described, no heat spreaders are necessary. Also, the solder layer can have a thickness that does not cause any cracks. The semiconductor device thus has sufficient packaging density to make the device compact enough. In addition, at least the soldering process of the heat spreader can be omitted. Thus, production cost of the semiconductor device can greatly be saved.

[0059] As shown in FIGURES 15-19, a number of preferred patterns of the lands 144 can be used to accurately position the semiconductor chips 66 thereon, as described below.

[0060] The semiconductor chips 66 are accurately positioned on the lands 144 so that the substrate 72 can be compact enough. The illustrated patterns in FIGURES 15-19 are applied in a soldering manner as part of the foregoing reflow soldering method. A conventional reflow soldering method typically needs several mounting tools to position the semiconductor chips on the lands. However, the method using the patterns does not require such a tool and thus is quite simple and cost saving. The patterns are specifically suitable for semiconductor chips which have rectangular or square shapes.

[0061] FIGURE 15 illustrates a preferred pattern of the land 144 that has four positioning or alignment corners 150 on lines 152, which include diagonal lines of the semiconductor chip (i.e., FET 66) in this embodiment. As shown in FIGURE 19, the land 144 is formed on the substrate 72. The solder layer 146, which is cream solder or half-solid solder as noted above, is applied on the land 144 so that the solder 146 exactly spreads over the area of the land 144. The semiconductor chip 66 is placed on the solder layer 146. In the illustrated arrangement, four corners or peaked portions of the semiconductor chip 66 are confined or trapped in the respective positioning corners 150 of the land pattern. That is, the corners 150 of the land 144 are disposed in close proximity to the corners of the semiconductor chip 66. The closer the positioning corners

150 of the land 144 are to the corners of the semiconductor chip 66, the more accurately the semiconductor chip 66 is positioned.

[0062] The land pattern also has four extended areas 154 along four sides of the semiconductor chip 66. In other words, the positioning corners 150 are the closest portions of the land 144 to the corners of the semiconductor chip 66. Further, the entire area of the land 144 is larger than the entire area of the semiconductor chip 66, and the area of the land 144 generally shrinks toward the corners of the semiconductor chip 66. Each extended area 154 in this pattern generally has a square configuration.

[0063] The extended areas 154 are useful to expand the entire area of the solder layer 146 that abuts on the land 144 and to allow bubbles in paste of the solder 146 to escape. The paste is employed to easily join the solder 146 with the land 144 and with the semiconductor chip 66; however, the paste may contain flux. Because the solder 146 is heated in the aforenoted reflow furnace, the flux can grow to bubbles and can make voids between the semiconductor chip 66 and the land 144. The extended areas 154 aid the bubbles to rapidly escape from the in-between areas. Because of the extended areas 154, substantially no voids can be made, and the land 144, the solder 146 and the semiconductor chip 66 can strictly join with each other. This has been verified experimentally. The wider the extended areas 154, the easier the bubbles escape inasmuch as the areas 154 do not affect the compact nature of the semiconductor device 52.

[0064] FIGURE 16 illustrates a modified pattern of the land 144. Two positioning corners 150 are made on a line 152 including one of the diagonal lines of the semiconductor chip 66 in this arrangement. This arrangement can also confine at least two of the corners of the semiconductor chip 66 and is sufficient to accurately position the semiconductor chip 66 on the land 144. Because the rest of the corners of the land 144 do not form the positioning areas, the extended areas 154 can extend wider than the pattern of FIGURE 15 and thus bubbles in the paste can escape easier than the pattern of FIGURE 15.

[0065] The extended areas 154 can take any configurations. For example, FIGURE 17 illustrates another modified pattern of the land 144. The pattern in this arrangement has four positioning corners 150 similar to the pattern shown in FIGURE 15 but has round or arc shaped extended areas 154.

[0066] FIGURE 18 illustrates a further modified pattern of the land 144. This pattern has two positioning corners 150 similar to the pattern shown in FIGURE 16 but has a round shape or generally circular shape.

[0067] Any configuration of the semiconductor chip 66 can be used with the positioning corners 150 of the land 144 inasmuch as the configuration has at least one diagonal line. That is, the configurations can include, for example, any rectangular and square shapes. The positioning corners 150 of the land 144 are particularly effective with such semiconductor chips 66 that have at least a side whose length is longer than approximately 2.5 millimeters. If the semiconductor chip has a rectangular shape, at least a length of a shorter side thereof is longer than approximately 2.5 millimeters. This is because the size of a larger size of the semiconductor chip 66 normally needs a margin of the land 144 that can exceed an allowable range in which the semiconductor chip 66 can be offset from a preset position. If a large offset from the preset position would occur, wires which are bonded to the wire bonding pads in a following wire bonding process could deviate from normal positions. However, the positioning corners 150 configured in accordance with the present invention can precisely confine the corners of the semiconductor chip 66 in a preset normal position.

[0068] The sufficient extended areas 154 of the land 144 are particularly effective with a power control semiconductor chip 66 because creation of voids can be extremely reduced. If a plurality of voids are created in the solder or the junction thereof with the semiconductor chip 66, resistance can greatly increase. Since a relatively large current flows through the power controlling semiconductor chip, the increase of the resistance can be greater and much power loss can occur. To the contrary, however, because of the extreme reduction of the voids in this arrangement, such a drawback cannot occur even with the power controlling semiconductor chip 66.

[0069] FIGURE 20 illustrates steps of an exemplified reflow soldering method in which the land patterns of FIGURES 15-19 can be applied. Electronic parts other than the semiconductor chips 66 are joined to the substrate 72 in this exemplified method. At a step S11, a chip mounter and a part mounter or a unified chip and part mounter mounts the semiconductor chips 66 and the parts onto each predetermined location on the substrate 72. The cream solder 146 is previously applied on the respective lands 144. Then, the substrate 72 is put into the reflow furnace at a step S12 to harden the cream

solder 146 by the hot blast. Because of the positioning corners 150 of the land patterns, no tool is necessary to keep the semiconductor chips 66 at the accurate positions in this improved manner.

[0070] The semiconductor chips 66 can of course be joined to the lands 144 in other methods. For instance, FIGURE 21 illustrates another method using the reflow furnace and die bonders. At a step S21, a part mounter mounts parts onto each predetermined location on the substrate 72. The cream solder 146 is previously applied at the respective portions of the parts which are soldered. The substrate 72 is put into the reflow furnace at a step S22 to fix the parts at the locations. At a next step S23, a die bonder A is used to join a first type of semiconductor chip or chips A to the substrate 72. The die bonder A bonds or joins only the first type of the semiconductor chips A. At a step S24, another die bonder B joins a second type of semiconductor chip or chips B to the substrate 72. In the same manner, at a step S25, a further die bonder C bonds a third type of semiconductor chip or chips C to the substrate 72. As such, further die bonders are used to join further types of semiconductor chips to the substrate 72 in due order. This method requires multiple die bonders corresponding to the respective types of semiconductor chips. However, the semiconductor chips can be mounted precisely onto the desired positions without any mounting tool.

[0071] FIGURES 22-26 illustrate a further method using the reflow furnace and a mounting tool. As shown in FIGURE 22, at a step S31, the part mounter mounts parts 160 onto each predetermined location on the substrate 72 as shown in FIGURES 23-25. The cream solder 146 is previously applied at the respective portions of the parts which are soldered. At a next step S32, a mounting tool 162 is set for positioning the semiconductor chips 66 at predetermined locations. The tool 162 has windows 164 through which the semiconductor chips 66 can be mounted. The chip mounter, at the step S32, mounts the semiconductor chips 66 onto the cream solder 146 applied on the lands 144 through the windows 164. Weights 166 are placed on the respective semiconductor chips 66. At a step S34, the substrate 72 with the semiconductor chips 66 and the parts 160 are put in the reflow furnace to fix to the substrate 72 by the hot blast. In this step S34, the tool 162 advantageously prevents the semiconductor chips 66 from slipping off the preset positions. The weights also are useful to prevent voids from being generated in

the solder 146 or to expedite the bubbles to escape from the solder 146 in the step S34. At a last step S35, the tool 162 and the weights 166 are detached.

[0072] FIGURE 26 illustrates a complete semiconductor device 52. Although the tool 162 and the weights 166 are necessary in this method, the entire semiconductor chips 66 and the electronic parts 160 can be simultaneously affixed to the substrate 72.

[0073] The foregoing description is that of preferred constructions and methods having certain features, aspects and advantages in accordance with the present invention. Various changes and modifications may be made to the above-described arrangements without departing from the spirit and scope of the invention, as defined by the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising a substrate, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer only through which the semiconductor chip is joined with the land, and a synthetic resin covering the land, the solder layer and the semiconductor chip on the substrate.

2. The semiconductor device as set forth in Claim 1, wherein a coefficient of expansion of the synthetic resin is generally less than a coefficient of expansion of the substrate or a coefficient of expansion of the land.

3. The semiconductor device as set forth in Claim 1, wherein the substrate comprises aluminum.

4. The semiconductor device as set forth in Claim 3, wherein a coefficient of expansion of the synthetic resin is generally less than a coefficient of expansion of aluminum.

5. The semiconductor device as set forth in Claim 4, wherein the coefficient of the linear expansion of the synthetic resin is generally less than approximately 23 ppm/°K.

6. The semiconductor device as set forth in Claim 3, wherein the land comprises copper.

7. The semiconductor device as set forth in Claim 3, wherein the synthetic resin includes epoxide.

8. The semiconductor as set forth in Claim 1, wherein a coefficient of expansion of the synthetic resin is generally less than one of a coefficient of expansion of the substrate and a coefficient of expansion of the land, and is generally greater than the other one of the coefficient of expansion of the substrate and the coefficient of expansion of the land.

9. The semiconductor as set forth in Claim 8, wherein the coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the substrate and is greater than the coefficient of expansion of the land.

Sub C2

10. The semiconductor as set forth in Claim 8, wherein the coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the land and is greater than the coefficient of expansion of the substrate.

11. The semiconductor as set forth in Claim 8, wherein the substrate comprises aluminum.

12. The semiconductor device as set forth in Claim 11, wherein the coefficient of the expansion of the synthetic resin is generally less than a coefficient of expansion of aluminum.

13. The semiconductor device as set forth in Claim 1, wherein the semiconductor chip defines at least two corners positioned generally opposite to each other, the land defines at least two corners in proximity to the corners of the semiconductor chip, and the corners of the land generally confine the corners of the semiconductor chip therein.

14. The semiconductor device as set forth in Claim 1, wherein the semiconductor chip controls electric power.

15. The semiconductor device as set forth in Claim 14, wherein the semiconductor chip controls power of an electric motor arranged to drive an electric vehicle.

16. A semiconductor device comprising a substrate, a land formed on the substrate, a semiconductor chip mounted on the land, a solder layer joining the semiconductor chip with the land, the semiconductor chip defining at least two corners positioned generally opposite to each other, the land defining at least two corners disposed in proximity to the corners of the semiconductor chip, the corners of the land generally confining the corners of the semiconductor chip therein.

17. The semiconductor device as set forth in Claim 16, wherein the corners of the land are the closest portions to the corners of the semiconductor chip.

18. The semiconductor device as set forth in Claim 16, wherein the semiconductor chip is generally configured as a rectangular shape, and the corners of the semiconductor chip are positioned on a diagonal line of the rectangular shape.

19. The semiconductor device as set forth in Claim 18, wherein the semiconductor chip defines four corners, and the land defines four corners corresponding to the corners of the semiconductor chip.

20. The semiconductor device as set forth in Claim 18, wherein at least a length of a shorter side of the rectangular shape is longer than approximately 2.5 millimeters.

21. The semiconductor device as set forth in Claim 16, wherein the land is generally configured as a rectangular shape except for the corners.

22. The semiconductor device as set forth in Claim 16, wherein the land is generally configured as a round shape except for the corners.

23. The semiconductor as set forth in Claim 16, wherein an area of the land is larger than an area of the semiconductor chip, and the area of the land generally shrinks toward the corners of the semiconductor chip.

24. The semiconductor as set forth in Claim 16, wherein an area of the land is larger than an area of the semiconductor chip, and the area of the land generally expands from the corners of the semiconductor chip.

25. The semiconductor device as set forth in Claim 16, wherein the semiconductor chip controls electric power.

26. The semiconductor device as set forth in Claim 16, wherein the semiconductor chip is joined with the land in a reflow soldering method.

27. A method for joining a semiconductor chip to a substrate comprising forming a land on the substrate, soldering the semiconductor chip directly to the land, and covering the land and the semiconductor chip with a synthetic resin.

28. The method as set forth in Claim 27, wherein a coefficient of expansion of the synthetic resin is set generally less than a coefficient of expansion of the substrate or a coefficient of expansion of a land.

29. The method as set forth in Claim 27, wherein a coefficient of expansion of the synthetic resin is set generally less than one of a coefficient of expansion of the substrate or a coefficient of expansion of the land and is generally greater than the other one of the coefficient of expansion of the substrate or the coefficient of expansion of the land.

30. The method as set forth in Claim 29, wherein the coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the substrate and is greater than the coefficient of expansion of the land.

31. The method as set forth in Claim 29, wherein the coefficient of expansion of the synthetic resin is less than the coefficient of expansion of the land and is greater than the coefficient of expansion of the substrate.

32. The method as set forth in Claim 27 additionally comprising forming positioning portions for the semiconductor chip on the land, and positioning the semiconductor chip at the positioning portions.

SEMICONDUCTOR DEVICE FOR POWER CONTROL

Abstract of the Disclosure

A semiconductor device for power control includes a substrate made of aluminum. Lands of copper are formed on the substrate. Semiconductor chips, such as FETs, are mounted on the lands. The semiconductor chips are joined with the lands only through solder layers. A synthetic resin, which includes epoxide, covers the lands, the solder layers and the semiconductor chips on the substrate. Preferably, a coefficient of expansion of the synthetic resin is generally less than a coefficient of expansion of the substrate or a coefficient of expansion of the lands. Each semiconductor chip defines at least two corners positioned generally opposite to each other. Each land defines at least two corners disposed in proximity to the corners of the semiconductor chip. The corners of the land generally confine the corners of the semiconductor chip therein.

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111901

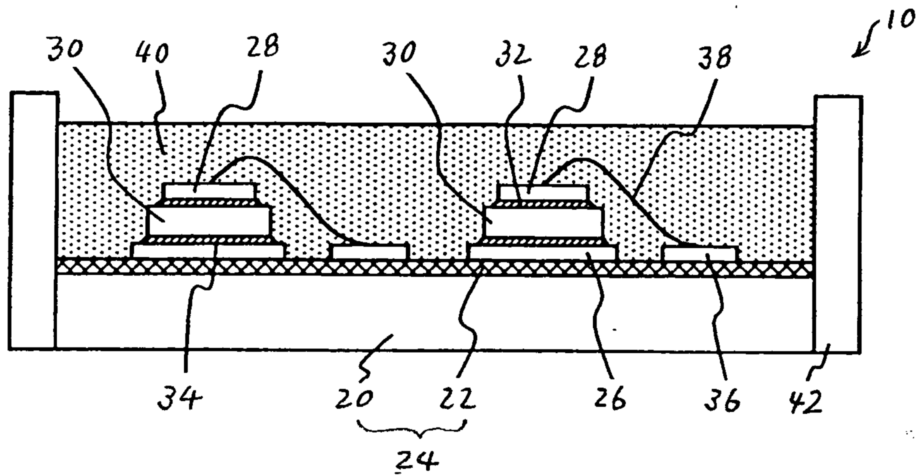


FIGURE 1

PRIOR ART

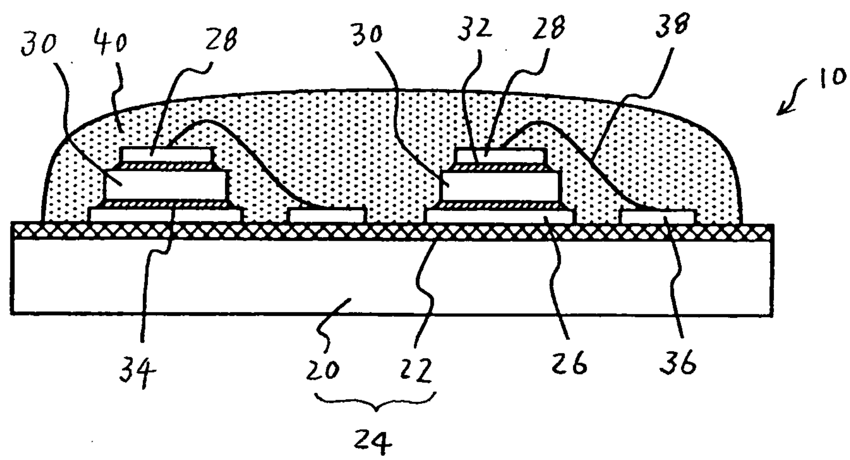


FIGURE 2

PRIOR ART

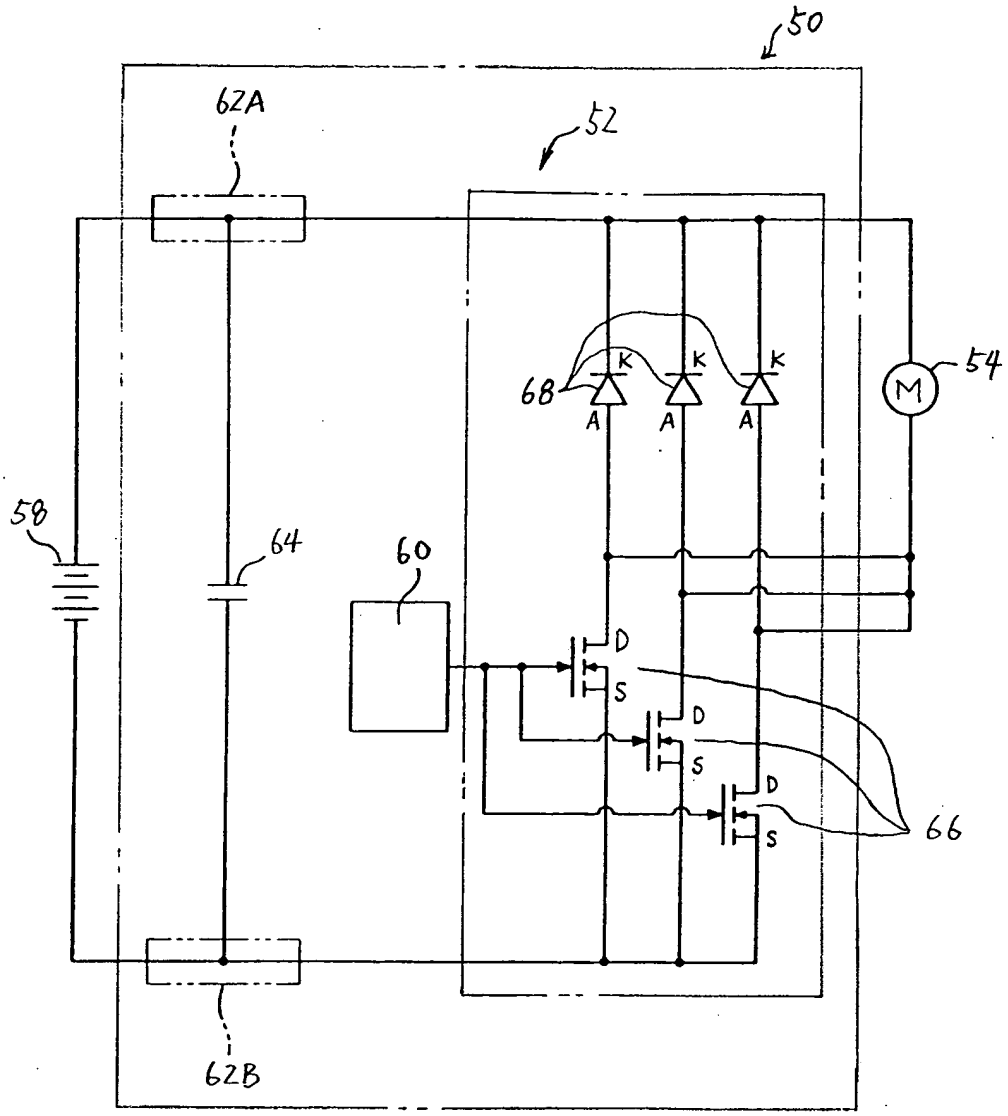
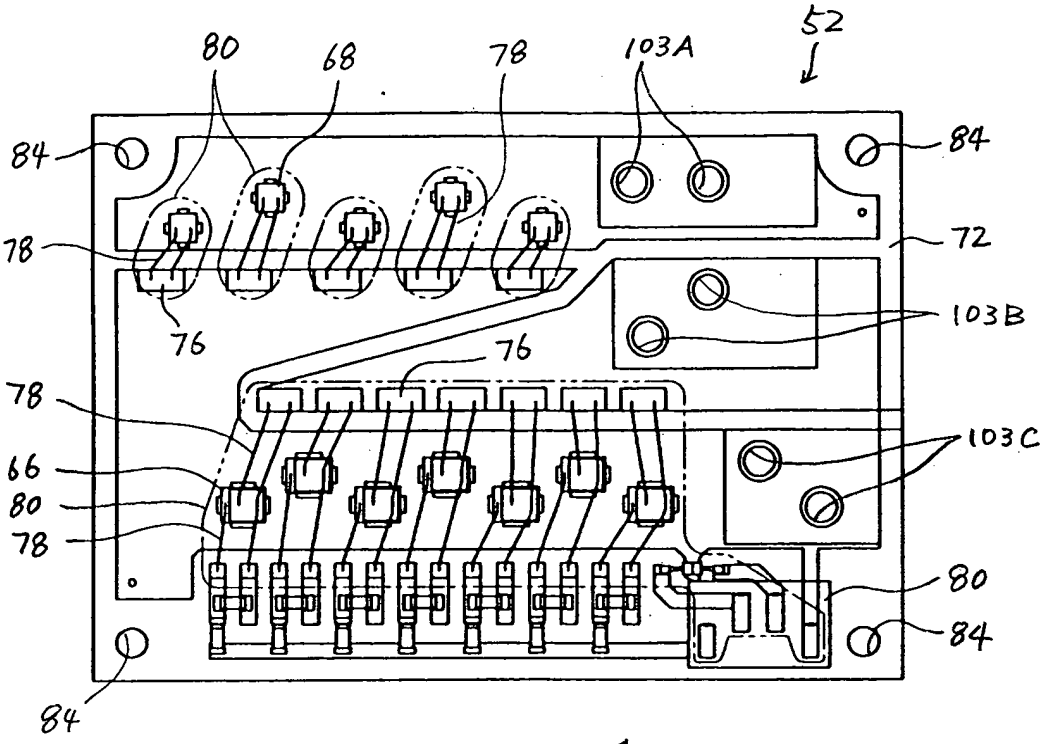


FIGURE 3



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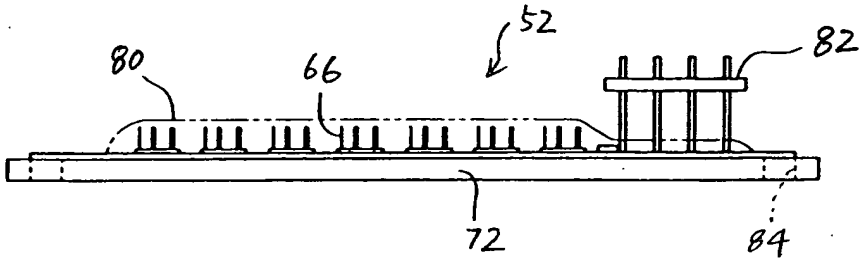

FIGURE 5

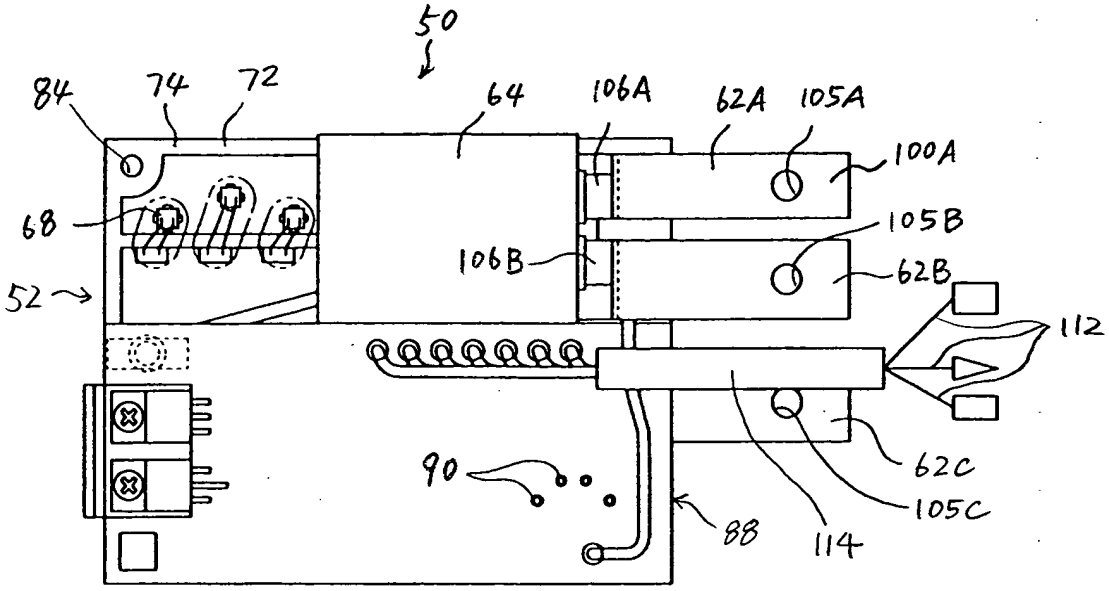

FIGURE 6

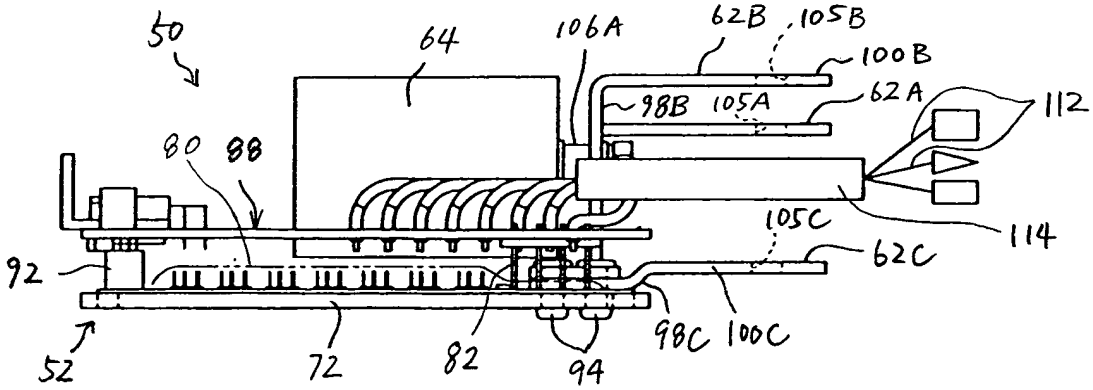

FIGURE 7

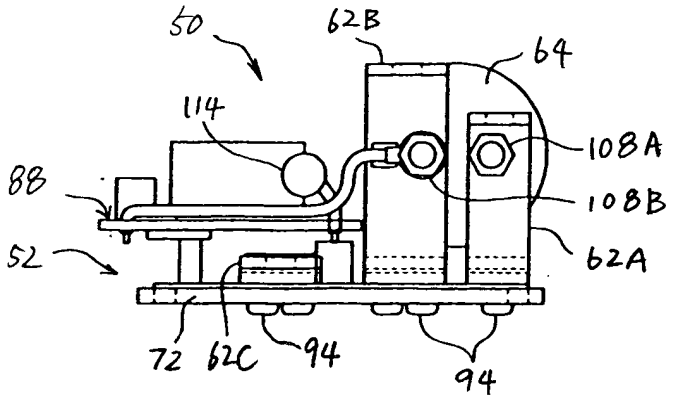

FIGURE 8

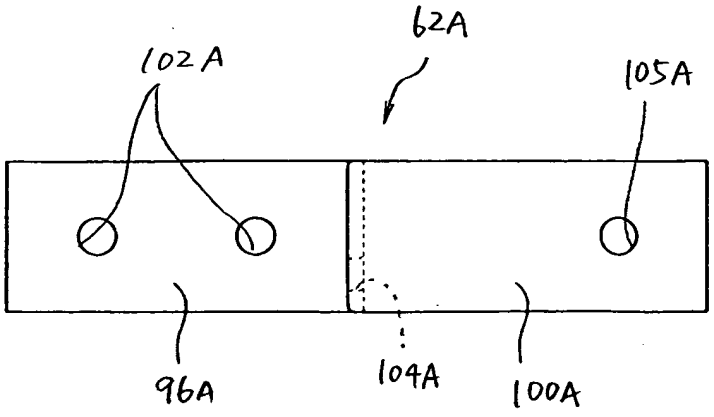

FIGURE 9

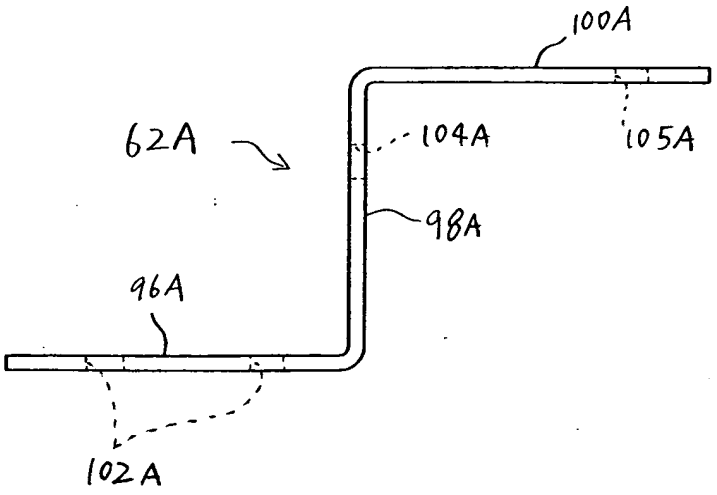

FIGURE 10

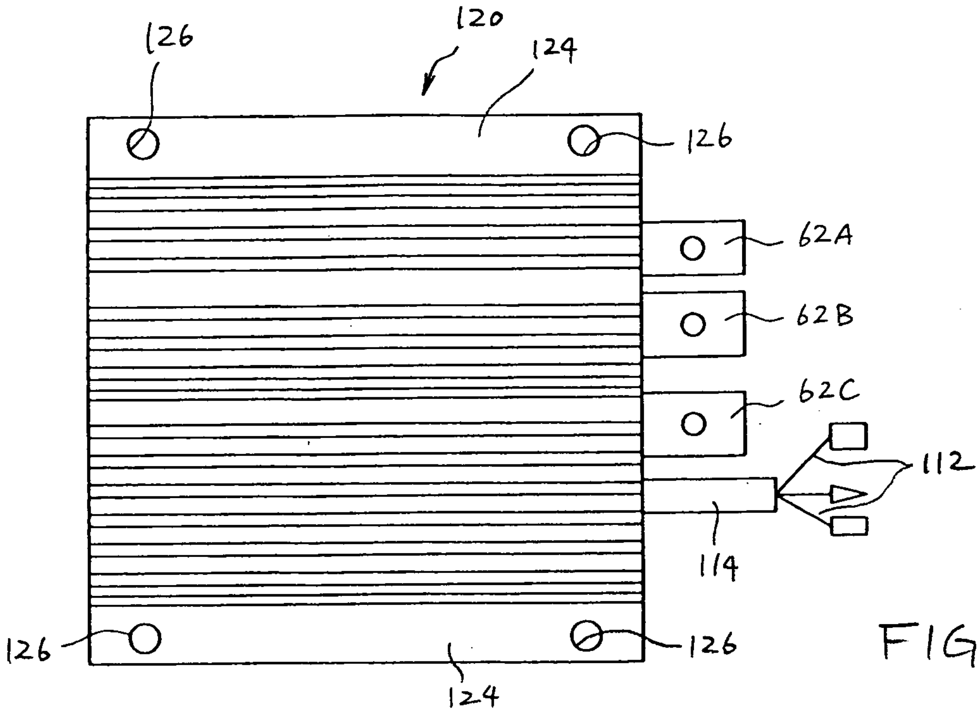

FIGURE 11

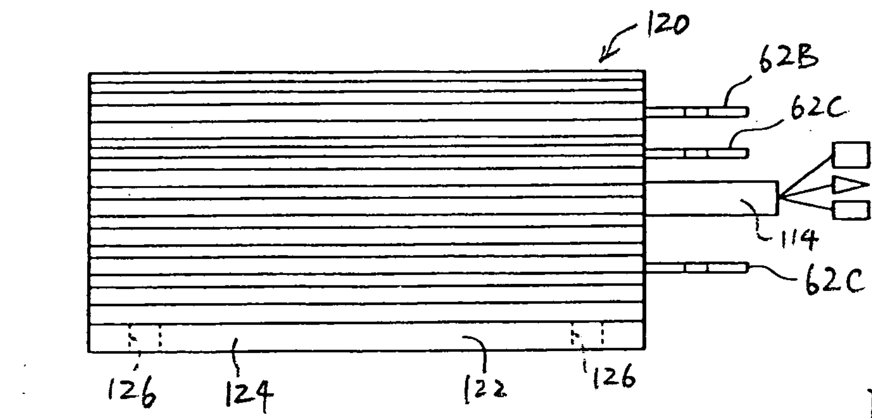

FIGURE 12

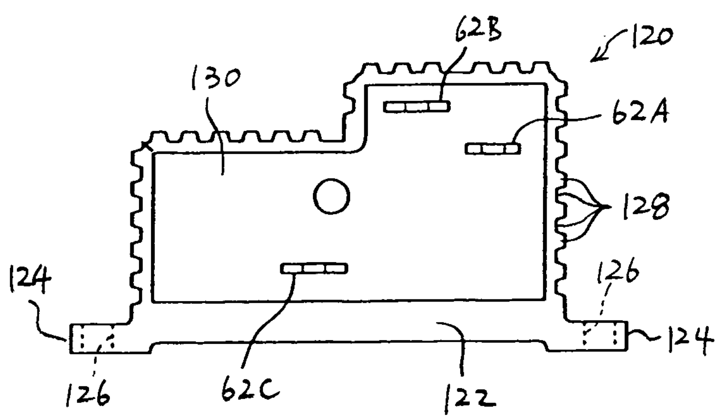

FIGURE 13

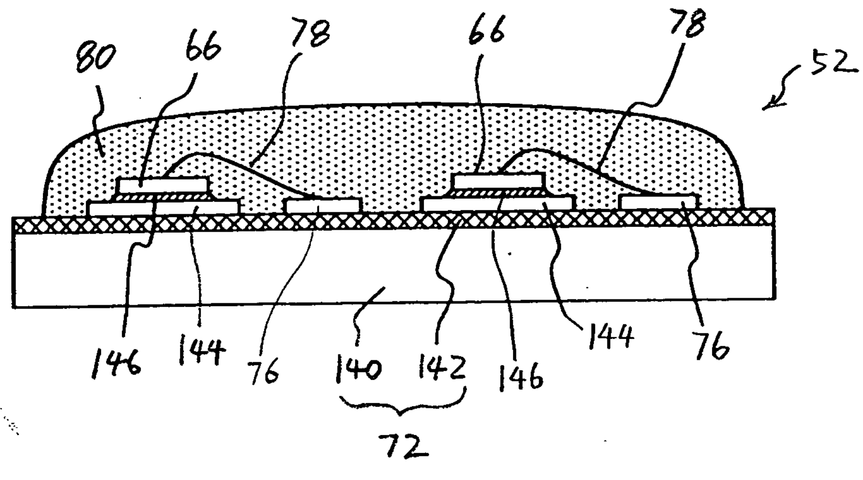

FIGURE 14

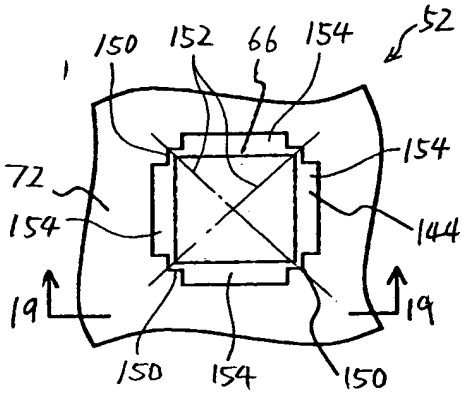

FIGURE 15

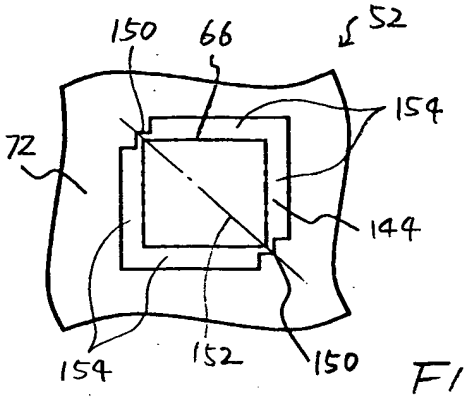

FIGURE 16

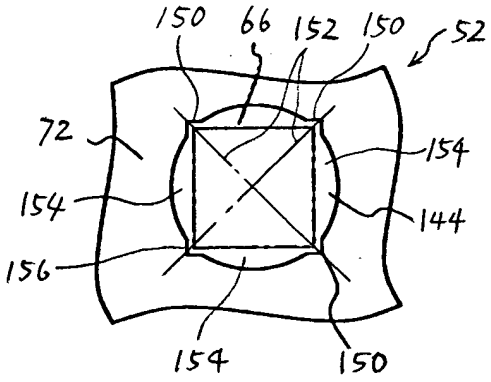

FIGURE 17

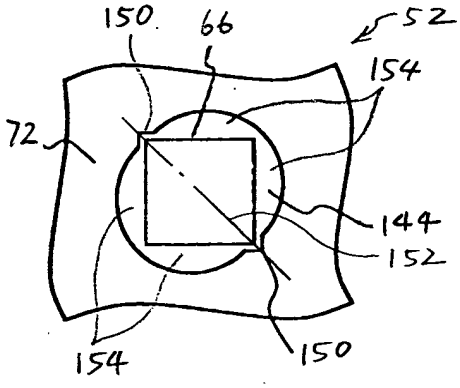

FIGURE 18

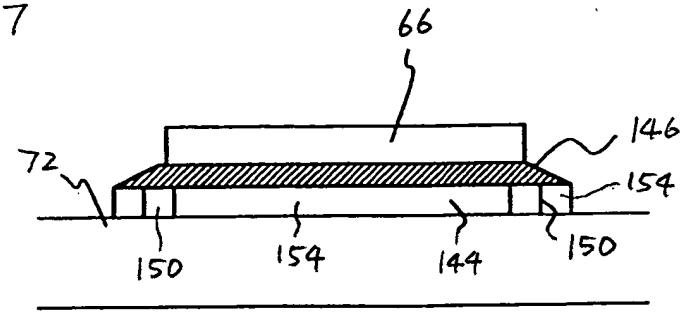

FIGURE 19

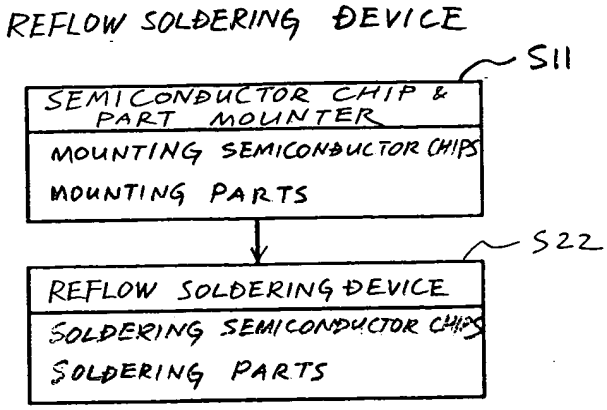

FIGURE 20

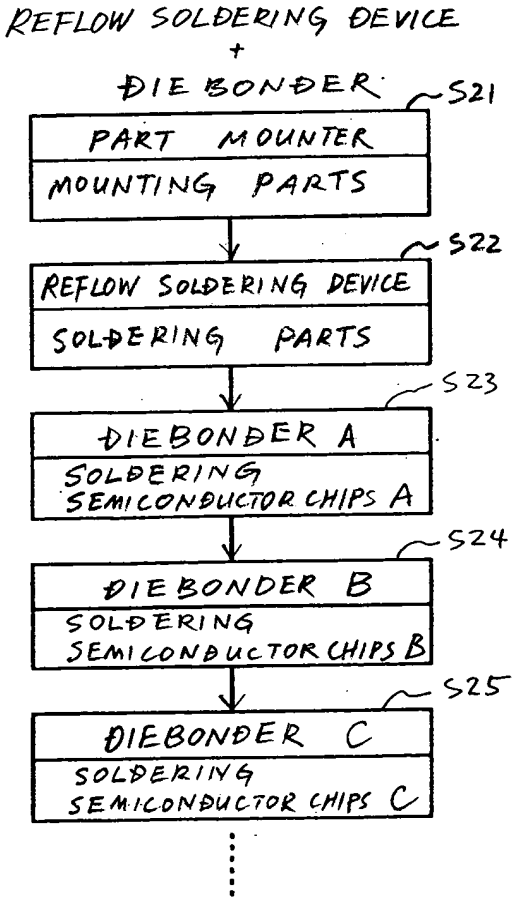

FIGURE 21

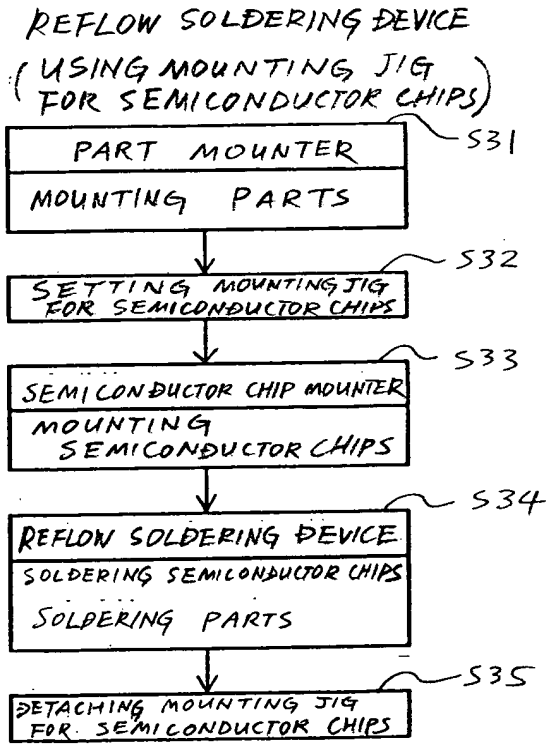

FIGURE 22

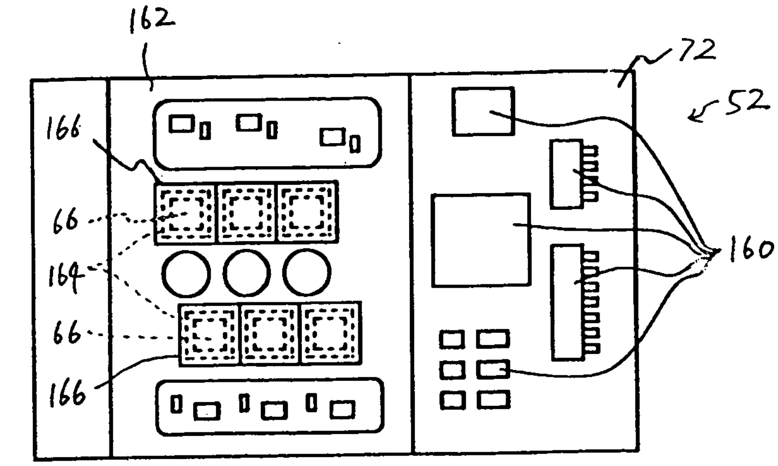

FIGURE 23

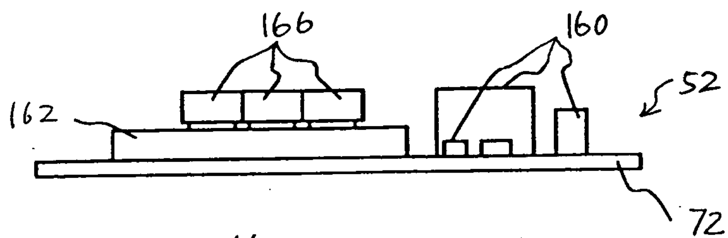

FIGURE 24

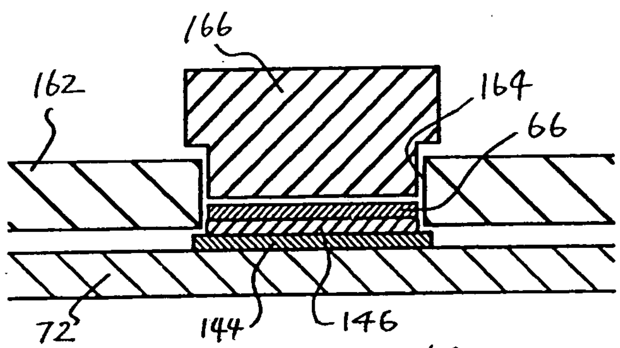

FIGURE 25

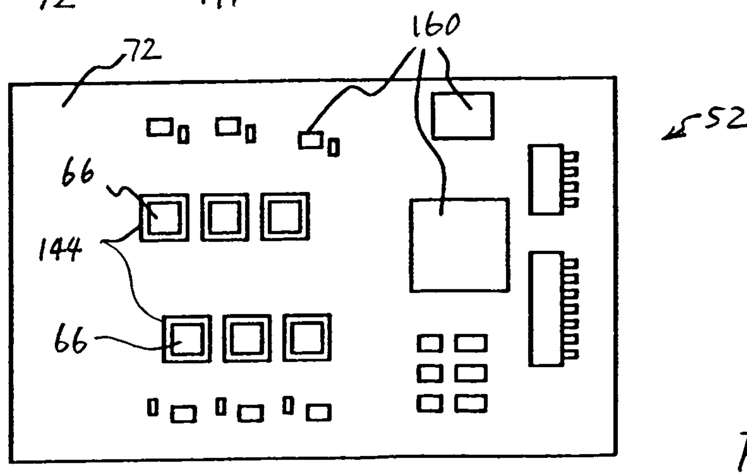

FIGURE 26

```
Set      Items   Description
S1      208307   POWER(2N)CONTROL?
S2     2344145   SUBSTRAT? OR WAFER?
S3      836681   DIELECTRIC? OR INSULAT?(2N)LAYER?
S4       30939   BASE()METAL?
S5      423742   LAND? ?
S6     3303421   COPPER OR CU OR AL OR ALUMINIUM
S7      245741   FET? ? OR FIELD()EFFECT()TRANSISTOR?
S8      241100   SYNTHETIC(2N)RESIN? OR EPOXIDE?
S9       63870   COEFFICIENT(3N)EXPANSION?
S10     137377   SOLDER
S11          8   S2 AND S5 AND S10 AND S8
S12          8   RD (unique items)
S13          0   S1 AND S6 AND S5 AND S8
S14         14   S1 AND S6 AND S5
S15         14   S14 NOT S12
S16          0   S7 AND S5 AND S8
S17        341   S8 AND S5
S18          5   S17 AND COEFFICIENT?
S19          5   RD (unique items)
S20          4   S19 NOT S12
S21       2059   S2 AND MOUNT? AND S5
S22         29   S9 AND S21
S23         29   RD (unique items)
S24         29   S23 NOT (S12 OR S15 OR S18)
? show
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12/9/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

04604104 **Image available**
ELECTRONIC COMPONENT FOR SURFACE MOUNTING

PUB. NO.: 06-276004 [JP 6276004 A]
PUBLISHED: September 30, 1994 (19940930)
INVENTOR(s): SHIIBA KENGO
HARADA YASUHIKO
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 05-058222 [JP 9358222]
FILED: March 18, 1993 (19930318)
INTL CLASS: [5] H01P-001/205; H01G-001/14; H01P-001/30; H05K-001/11
JAPIO CLASS: 44.1 (COMMUNICATION -- Transmission Circuits & Antennae); 42.1 (ELECTRONICS -- Electronic Components)
JOURNAL: Section: E, Section No. 1651, Vol. 18, No. 687, Pg. 35, December 26, 1994 (19941226)

ABSTRACT

PURPOSE: To provide the electronic component for surface mounting which is high in yield and reducible in size, superior in durability, operability, productivity, heat resistance, and reliability, and securely mounted on electronic equipment, etc., and facilitates the soldering of a terminal, has the high mechanical strength of the terminal to an external force, and absorbs an external shock, etc.

CONSTITUTION: The electronic component for surface mounting is equipped with a **substrate** 1 as its main body, a **land** 2 formed on the **substrate** 1, the terminal 7 as the signal input/output part of the electronic component for surface mounting joined with the **land** 2, and **solder** 8 for fixing the **land** 2 to the terminal 7; and a projection part is formed at at least one of the fixation- side tip part of the terminal and both side parts in the length direction and the **solder** 8 and/or the tip projection part 7a of the terminal 7 which projects from the **solder** 8 and its peripheral part are coated with a **synthetic resin** layer 9.

12/9/7 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014869379 **Image available**
WPI Acc No: 2002-690085/200274
XRAM Acc No: C02-194998
XRPX Acc No: N02-544314
Semiconductor device, used in motor controller of electric cart, has solder layer through which semiconductor chip is joined with copper land
Patent Assignee: YAMAHA MOTOR CO LTD (YMHA); MORITA K (MORI-I); MURAI T (MURA-I); YOSHIKAWA T (YOSH-I)
Inventor: MORITA K; MURAI T; YOSHIKAWA T
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020074651	A1	20020620	US 200122297	A	20011212	200274	B
JP 2002184791	A	20020628	JP 2000379567	A	20001214	200274	
JP 2002184907	A	20020628	JP 2000379569	A	20001214	200274	

JP 2002262593 A 20020913 JP 200152498 A 20010227 200276

Priority Applications (No Type Date): JP 200152498 A 20010227; JP 2000379567 A 20001214; JP 2000379569 A 20001214

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020074651	A1		18	H01L-023/34	
JP 2002184791	A		5	H01L-021/52	
JP 2002184907	A		3	H01L-023/28	
JP 2002262593	A		6	H02P-007/00	

Abstract (Basic): US 20020074651 A1

NOVELTY - Semiconductor chips (66) are joined with copper **lands** (144) formed on an aluminum **substrate** (72) through a soldering layer (146). An **epoxide synthetic resin** (80), which covers the **land** , **solder** layer and the semiconductor chip, has coefficient of expansion less than that of the **substrate** or the **land** .

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for joining semiconductor chip to **substrate** .

USE - Semiconductor device for use in motor controller of electrically operated vehicle such as electric golf cart.

ADVANTAGE - The device has high packaging capacity so making it highly compact. The device has high accuracy of positioning of semiconductor chips without requiring expensive heat spreaders.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic front view of the semiconductor device.

Semiconductor chip (66)

Aluminum **substrate** (72)

Epoxide synthetic resin (80)

Copper **land** (144)

Soldering layer (146)

pp; 18 DwgNo 14/26

Title Terms: SEMICONDUCTOR; DEVICE; MOTOR; CONTROL; ELECTRIC; CART; **SOLDER** ; LAYER; THROUGH; SEMICONDUCTOR; CHIP; JOIN; COPPER; **LAND**

Derwent Class: A85; L03; U11

International Patent Class (Main): H01L-021/52; H01L-023/28; H01L-023/34; H02P-007/00

International Patent Class (Additional): H01L-023/12; H01L-023/40; H01L-025/07; H01L-025/18; H05K-007/20

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A12-E07C; L04-C17A; L04-C20A; L04-C21

Manual Codes (EPI/S-X): U11-D02B

Polymer Indexing (PS):

<01>

001 018; P0464-R D01 D22 D42 F47

002 018; ND01; Q9999 Q7476 Q7330; Q9999 Q7443 Q7421 Q7330; K9416

?

15/9/12 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015143663 **Image available**
WPI Acc No: 2003-204190/200320
XRPX Acc No: N03-162717
Power semiconductor module for electric power control **, has high thermal conductance electric insulation material pinched in intermediate position of gap between adjacent** lands **to which chip component is soldered**
Patent Assignee: SANSHA DENKI SEISAKUSHO KK (SAOD)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2002343935	A	20021129	JP 2001141057	A	20010511	200320	B

Priority Applications (No Type Date): JP 2001141057 A 20010511
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2002343935	A		4	H01L-025/07	

Abstract (Basic): JP 2002343935 A
NOVELTY - A chip component (4) is soldered (8) to the **lands** (5) of a **copper** circuit (3) formed on metal substrate through an electric insulation layer. A high thermal conductance electric insulation material is pinched in the intermediate position of the gap between the opposing **lands** .
USE - For electric **power control** .
ADVANTAGE - The temperature of the chip component is restrained low by the high thermal conductance heat insulation material, thereby improving durability and reliability of the semiconductor module.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the semiconductor module.
pp; 4 DwgNo 1/4
Title Terms: POWER; SEMICONDUCTOR; MODULE; ELECTRIC; POWER; CONTROL; HIGH; THERMAL; CONDUCTING; ELECTRIC; INSULATE; MATERIAL; PINCH; INTERMEDIATE; POSITION; GAP; ADJACENT; **LAND** ; CHIP; COMPONENT; SOLDER
Derwent Class: U11; U24
International Patent Class (Main): H01L-025/07
International Patent Class (Additional): H01L-025/18
File Segment: EPI
Manual Codes (EPI/S-X): U11-D01C6; U24-E
?

24/9/4 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04292659 JICST ACCESSION NUMBER: 99A0867828 FILE SEGMENT: JICST-E
The most suitable design of the lands **for chip component soldering utilizing the FEM analysis.**
NARUSE TOSHIMICHI (1); SUGITA HIROKAZU (1); SAKAMOTO NORIAKI (1); SHIMIZU HISASHI (1)
(1) SANYO Electr. Co., Ltd.
Maikuro Erekutoronikusu Shinpojiumu Ronbunshu, 1998, VOL.8th, PAGE.261-264, FIG.8, TBL.3
JOURNAL NUMBER: X0060AAN
UNIVERSAL DECIMAL CLASSIFICATION: 621.315.68 621.382.08 681.3:519.6
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
DESCRIPTORS: printed board; soldering; reliability analysis; finite element method; surface **mount** technology; cycle life; heat cycle; stress concentration; thermal stress analysis; thermal **expansion coefficient** ; stress relaxation; optimum design
IDENTIFIERS: temperature cycling
BROADER DESCRIPTORS: **substrate** (plate); plate classified by application; plate(material); electric apparatus and parts; parts; brazing; bonding and joining; analysis; approximation method; high density packaging; packaging(**mounting**); lifetime; cycle; phenomena in strength of material; phenomenon; stress analysis; **expansion coefficient** ; coefficient; relaxation phenomenon; design
CLASSIFICATION CODE(S): NA05050Z; NC03040G; JE02000J

24/9/7 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06849724 **Image available**
SEMICONDUCTOR ELEMENT HOUSING PACKAGE AND **MOUNTING** STRUCTURE THEREFOR

PUB. NO.: 2001-077224 [JP 2001077224 A]
PUBLISHED: March 23, 2001 (20010323)
INVENTOR(s): MAEDA KAZUTAKA
NAKAGAWA SHOICHI
KOKUBU MASAYA
AZUMA MASAHIKO
APPLICANT(s): KYOCERA CORP
APPL. NO.: 11-245344 [JP 99245344]
FILED: August 31, 1999 (19990831)
INTL CLASS: H01L-023/12

ABSTRACT

PROBLEM TO BE SOLVED: To provide a semiconductor element housing package and a **mounting** structure therefor, which are capable of maintaining rigid and stable connection with an external circuit board over a long period of time and forming **lands** at a high density.

SOLUTION: A semiconductor element housing package A includes a metallized wiring layer 2 for electrical connection with a semiconductor element 4 formed on the surface of a ceramic insulating **substrate** 1, and metallized

lands 3. For **mounting** the package A on an external circuit board B, the **coefficient** of thermal **expansion** of the **substrate** 1 of the package A is set to 8-18 ppm/°C or less, a difference between its **coefficient** of thermal **expansion** and that of the element 4 is set to 12 ppm/°C or less, the Young's modulus is set to 50-150 GPa, and the difference between the **coefficient** of thermal **expansion** of the **substrate** 1 and that of an insulator 11 of the board B is set to 10 ppm/°C or less. As a result, superior connection reliability can be obtained, with the **lands** 3 being arranged at an interval x of 0.8 mm or less and a layer of conductors 10 interposed between the **lands** 3 and **lands** 12 of the board B having a thickness Y of 0.3 mm or less.

24/9/12 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO

04425725 **Image available**
MOUNTING METHOD FOR CAPACITOR

PUB. NO.: 06-069625 [JP 6069625 A]
PUBLISHED: March 11, 1994 (19940311)
INVENTOR(s): UEHARA AKIRA
APPLICANT(s): FUJITSU GENERAL LTD [000661] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-219922 [JP 92219922]
FILED: August 19, 1992 (19920819)
INTL CLASS: [5] H05K-001/18; H01G-004/12
JAPIO CLASS: 42.1 (ELECTRONICS -- Electronic Components)
JOURNAL: Section: E, Section No. 1562, Vol. 18, No. 318, Pg. 31, June 16, 1994 (19940616)

ABSTRACT

PURPOSE: To prevent a capacitor from being broken by a difference of thermal **expansion coefficient** by **mounting** a ceramic capacitor on an aluminum **substrate** or a printed wiring board through a flexible board.

CONSTITUTION: Solder print treatment is first performed for an electrode **land** part 4 of a flexible board 2. After an electrode part 10 of a ceramic capacitor 3 is **mounted** on the electrode **land** part 4 which is correspondingly provided to stride over an opening part 5 provided to a flexible board 2, soldering treatment is performed. After solder print treatment is performed for a required part of a copper foil pattern part 7 of an aluminum **substrate** or a printed board 1 and a connection **land** 9 of the flexible board 2 whereon the ceramic capacitor 3 is **mounted** is **mounted** on the copper foil pattern part 7, soldering treatment is carried out. Thereby, difference of thermal **expansion coefficient** between the ceramic capacitor 3 and the aluminum **substrate** or the printed wiring board 1 is absorbed by the flexible board 2.

24/9/22 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014007501 **Image available**
WPI Acc No: 2001-491715/200154
XRAM Acc No: C01-147803

XRPX Acc No: N01-363911

Surface mounting **type semiconductor light emitting device for liquid crystal display panel, has epoxy resin provided on front and rear sides of** substrate **for resin sealing of luminescent element**

Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE)

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 2001135860	A	20010518	JP 99315188	A	19991105	200154	B

Priority Applications (No Type Date): JP 99315188 A 19991105

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001135860	A		6	H01L-033/00	

Abstract (Basic): JP 2001135860 A

NOVELTY - The device includes a pair of electrodes (2,3) formed on the **substrate** (1). A luminescent element (4) **mounted** on **land** (2a) of electrode (2) is connected to electrode (3) by a wire (5). The resin sealing of luminescent element is performed by using an epoxy resin that is provided on both front and rear sides of the **substrate** .

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor light emitting device manufacturing method.

USE - For liquid crystal display panel for portable telephone.

ADVANTAGE - Since the epoxy resin is formed on both front and rear sides of the **substrate** , the peeling-off of resin from the **substrate** due to the different in thermal **expansion coefficient** by heating, is prevented and the **substrate** supports the luminescent element stably.

DESCRIPTION OF DRAWING(S) - The figure shows front view of semiconductor light emitting device.

Substrate (1)

Electrodes (2,3)

Land (2a)

Luminescent element (4)

Wire (5)

pp; 6 DwgNo 2/9

Title Terms: SURFACE; **MOUNT** ; TYPE; SEMICONDUCTOR; LIGHT; EMIT; DEVICE; LIQUID; CRYSTAL; DISPLAY; PANEL; EPOXY; RESIN; FRONT; REAR; SIDE; **SUBSTRATE** ; RESIN; SEAL; LUMINESCENT; ELEMENT

Derwent Class: A85; L03; U12

International Patent Class (Main): H01L-033/00

File Segment: CPI; EPI

Manual Codes (CPI/A-N): A99-A; L03-G05B; L04-E03

Manual Codes (EPI/S-X): U12-A01A1A

?

15/3,K/12 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015143663 **Image available**
WPI Acc No: 2003-204190/200320
XRPX Acc No: N03-162717
Power semiconductor module for electric power control **, has high thermal conductance electric insulation material pinched in intermediate position of gap between adjacent** lands **to which chip component is soldered**
Patent Assignee: SANSHA DENKI SEISAKUSHO KK (SAOD)
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Patent Family:

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Priority Applications (No Type Date): JP 2001141057 A 20010511
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... For electric **power control** .

...Title Terms: **LAND** ;